ABSTRACT OF THE DISCLOSURE

The present invention aims to reduce a waiting time of an information processing machine from reception of an interrupt request signal to an actual start of an interrupt process. The information processing machine includes a CPU that normally operates with a first clock. The machine also includes a circuit for generating a second clock which is faster than the first clock. Upon receiving the second clock, a clock switching circuit of the machine supplies the second clock to the CPU instead of the first clock in order to cause the CPU to operate with the second clock. When an interrupt control circuit of the machine receives the interrupt request signal, it supplies a start signal to the CPU and the second clock generating circuit so as to cause the CPU to start preparation for the interrupt process and to cause the second clock generating circuit to produce the second clock.